AMENDMENTS TO THE SPECIFICATION

Amend the paragraph starting at page 12, line 28, as follows:

In this case, the thin film transistor of this embodiment simultaneously etches the a-Si film 27, first SiNx film 28 and second SiNx film 29 respectively serving as a gate insulating film by using the pattern of the gate electrode 30 as a mask. As a result, as shown in the left side of Figure 2, the a-Si film 27, first SiNx film 28 and second SiNx film 29 are left at all ~~lower~~ portions beneath ~~of~~ the gate line 31 as ~~and~~ an unnecessary semiconductor layer ~~is left below the gate line 31 other than an a-Si island~~.

Amend the paragraph starting at page 16, line 19, as follows:

Then, as shown in Figure 5(d), the gate electrode 30 and gate line 31 are formed through photolithography. In case of this embodiment, the a-Si film 27, first SiNx film 28, and second SiNx film 29 are simultaneously etched by using the gate electrode 30 and gate line 31 as masks. As a result, because these films can be continuously etched through one-time lithography step, it is possible to greatly shorten the manufacturing process. In this case, by shortening the process, a TFT array is completed in which a ~~while an unnecessary~~ semiconductor layer remains not only in the a-Si island region under ~~around~~ the gate electrode 30 necessary as a TFT, but also in ~~on~~ the ~~lower~~ layer under ~~of~~ the gate line 31. To compensate for this, pursuant to the present invention, the gate is patterned as a protruded TFT portion, protruding from the gate line 31, with the protruded TFT portion having a base area near the gate line (near the drain electrode 26 in Figure 1) and an extended area beyond the base area (near the source electrode 25 in Figure 1). In this configuration, the drain electrode 26, serving as a signal electrode, crosses the base area of the protruded TFT portion. The drain

electrode 26 separates the extended area of the protruded TFT portion from the gate line 29, to prevent leakage currents. ~~However, b~~ Because the drain electrode 26 is patterned so as to stride/cross the root/base of the gate electrode 30 in the step shown in Figure 5(b), it is possible to prevent a potential from weakening due to crosstalk from an adjacent data line.